2183 #12 pay 7-6-04

Docket No.: 212005US2

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COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 09/919,859
Applicants: Hans Jurgen MATTAUSCH, et al.
Filing Date: August 2, 2001
For: MULTI-PORT CACHE MEMORY
Group Art Unit: 2188
Examiner: VITAL, P. M.

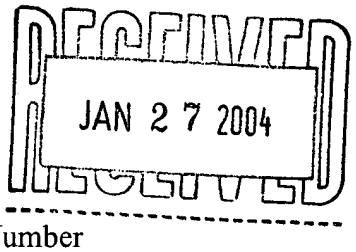
SIR:

Attached hereto for filing are the following papers:

INVENTOR DECLARATION (3 SETS OF 2 PAGES)

Our check in the amount of **$0.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time.

Respectfully submitted,



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DOCKET NO: 212005US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

HANS JURGEN MATTAUSCH, ET AL. : EXAMINER: VITAL, P. M.

SERIAL NO: 09/919,859 :

FILED: AUGUST 2, 2001 : GROUP ART UNIT: 2188

FOR: MULTI-PORT CACHE MEMORY :

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We, the inventors of the above-identified patent application, were a professor and students at Hiroshima University, respectively, when preparing said patent application. In preparing our patent application, we incorrectly surmised what constituted prior art to our invention. Therefore, we incorrectly identified Figures 1 and 2 of U.S. Patent application Serial No. 09/919,859 as prior art. The errors made in labeling originally Figures 1 and 2 as prior art were made without deceptive intent. The inventors, a professor and students at the university, were unaware of the legal meaning of the term prior art when they surmised what might be available.

The inventors note that the original purpose of Figures 1 and 2 was to explain the different between a multi-port cell cache and a cache based on multiple banks with one port-cell. The inventors now believe that there is no prior art corresponding to originally filed Figures 1 and 2. Therefore, Figures 1 and 2 have been amended to remove the conflict management circuit 60. Also, new Figures 11 and 12 have been added to correspond to

originally filed Figures 1 and 2. New Figures 11 and 12 show that simultaneous read accesses to the same cache address are possible for a multi-port cache constructed from multi-port-memory cells. Thus, new Figures 11 and 12 show a straight forward possibility for constructing a multi-port cache from multi-port memory cells. The inventors are unaware of any prior art which corresponds to Figures 11 and 12. In fact, the inventors note that multi-port caches were not conventionally used at the time of invention because a multi-port cache constructed from multi-port memory cell were uneconomical.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

January 4, 2004
Date

Hans Jürgen Mattausch
Dr. Hans Jurgen Mattausch, Inventor
Hiroshima-ken, JAPAN

Date

Koji Kishi, Inventor
Tokyo, JAPAN

Date

Nobuhiko Omori, Inventor
Oura-gun, JAPAN

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Date	Dr. Hans Jurgen Mattausch, Inventor Hiroshima-ken, JAPAN
January 5, 2004 Date	Koji Kishi Koji Kishi, Inventor Tokyo, JAPAN
Date	Nobuhiko Omori, Inventor Oura-gun, JAPAN

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Date	Dr. Hans Jurgen Mattausch, Inventor Hiroshima-ken, JAPAN
Date	Koji Kishi, Inventor Tokyo, JAPAN
January 5, 2004 Date	Nobuhiko Omori Nobuhiko Omori, Inventor Oura-gun, JAPAN

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